

Patent
10/039,284

IN THE CLAIMS:

Please cancel Claims 18-32.

Please amend Claim 1 as indicated.

1. (Currently Amended) A method of forming a power semiconductor device comprising the steps of:
 - A. providing a substrate of a first or second conductivity type;
 - B. forming a voltage sustaining region on said substrate by:
 - 1 a. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;
 - 2 b. etching at least one trench in the epitaxial layer with an etchant gas having a dopant species of the second conductivity type to form a doped surface layer in a portion of the epitaxial layer defining the trench walls;
 - 3 c. diffusing further into the epitaxial layer the dopant species located in said doped surface layer to form a doped epitaxial region adjacent to the trench and in the epitaxial layer;
 - 4 d. depositing a filler material in said trench to substantially fill said trench; and
 - C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.
2. (Original) The method of claim 1 wherein the step of depositing the filler material is performed before the step of diffusing the dopant species.
3. (Original) The method of claim 1 wherein the step of depositing the filler material is performed after the step of diffusing the dopant species.
4. (Original) The method of claim 1 wherein step (C) further includes the steps of:

Patent
10/039,284

forming a gate conductor above a gate dielectric region;
forming first and second body regions in the epitaxial layer to define a drift
region therebetween, said body regions having a second conductivity type;
forming first and second source regions of the first conductivity type in the first and
second body regions, respectively.

5. (Original) The method of claim 1 wherein said material filling the trench is
undoped polysilicon.

6. (Original) The method of claim 1 wherein said material filling the trench is a
dielectric material.

7. (Original) The method of claim 6 wherein said dielectric material is silicon
dioxide.

8. (Original) The method of claim 6 wherein said dielectric material is silicon
nitride.

9. (Original) The method of claim 1 wherein said dopant species is boron.

10. (Original) The method of claim 9 wherein said etchant gas is BCl₃.

11. (Original) The method of claim 1 wherein said dopant species is phosphorus.

12. (Original) The method of claim 11 wherein said etchant gas is PH₃.

13. (Original) The method of claim 4 wherein said body regions include deep
body regions.

Patent
10/039,284

14. (Original) The method of claim 1, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

15. (Original) The method of claim 1 wherein the etching step is performed by reactive ion etching.

16. (Original) The method of claim 4, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

17. (Original) The method of claim 1 wherein said power semiconductor device is selected from the group consisting of a vertical DMOS, V-groove DMOS, and a trench DMOS MOSFET, an IGBT, and a bipolar transistor.

18-32. (Canceled)